Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. - 7. (Cancelled)

8. (Currently Amended) Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, the circuit comprising a first and second asynchronous clock ~~domains~~ domain, wherein jitter elements are additionally insertable at predetermined portions of circuit boundaries between the first and second asynchronous clock ~~domains~~ domain, the jitter elements being representable as logical elements, the values of which are randomly set.

9. (Currently Amended) The system of claim 8, wherein the simulation is carried out on ~~cycle~~ a cycle level of a description of the electronic circuit.

10. (Original) The system of claim 8, wherein the jitter elements comprise delay elements for introducing predetermined timing delays ~~which is~~ which are randomly exercised.

11. (Original) The system of claim 8, wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

12. (Original) The system of claim 8, wherein the jitter elements are interactively inserted by a user.

13. (Original) The system of claim 8, wherein the jitter elements are automatically inserted using predetermined modules.

14. - 15. (Cancelled)